RAVENNA 2020 Webinar Series

AES67 & SMPTE ST 2110 Timing & Synchronization

Tue, June 9, 2020
15:00 h (CEST)

Daniel Boldt, Meinberg

Andreas Hildebrand, ALC NetworX

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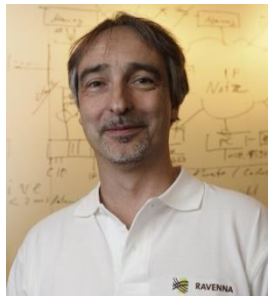
ALC NetworX

Your Host



Andreas Hildebrand, RAVENNA Technology Evangelist

- more than 25 years in the professional audio / broadcasting industry
- graduate diploma in computer science
- R&D, project & product management experience
- member of AES67 TG and ST2110 DG

ALC NetworX GmbH, Munich / Germany

- established 2008
- R&D center
- developing & promoting RAVENNA
- Partnerships with > 40 manufacturers

RAVENNA

- IP media networking technology
- designed to meet requirements of professional audio / broadcasting applications
- open technology approach, license-free
- fully AES67-compliant (*built-in*)

Daniel Boldt, Head of Software Development, Meinberg

- Diploma in Media Technology (Thesis done at ZDF, German television)
- 20 years experience with the development of synchronization products
- Main Topics: IEEE 1588, NTP, LANTIME and microSync Firmware platforms

MEINBERG
The Synchronization Experts.

MEINBERG, Bad Pyrmont / Germany

- established 1979
- Full-Depth Manufacturer of Time and Frequency Synchronization Equipment (R&D, Production, Sales & Marketing at a single location)
- Time and Sync solutions for all industries (Broadcast, Power, Telecom, Finance, etc..)
- Acquired PTP technology supplier Oregano Systems (Vienna) in 2019
- Active in various standardization bodies (IEEE, ITU, SMPTE, IETF,…)

Timing & Synchronization – General Requirements

- Media bit-transparency
  - → no sample rate conversion
  - → streams need to run on same media clock
- Concurrent operation of different sample rates on same network
- Determinable (low) end-to-end latency
- Time alignment between media streams
- Replacement for “house clock” distribution (word clock, black burst etc.)

⇨ Clock reassembly from stream data not appropriate
⇨ Distribution of master clock beats not sufficient
⇨ Common understanding of absolute time required (“wall clock”)

Timing & Synchronization – Accuracy Requirements

- Audio applications have highest time accuracy & precision demands:

  ⇨ Sample accurate alignment of streams (± ½ sample)
  - @ 48 kHz: ± 10 µs
  - @ 96 kHz: ± 5 µs
  - @ 192 kHz: ± 2.5 µs

  ⇨ "Distribution" of word clock reference (AES11 calls for ± 5% max jitter / wander):
  - @ 48 kHz: ± 1 µs
  - @ 96 kHz: ± 500 ns
  - @ 192 kHz: ± 250 ns

Synchronization & Media Clocks

- All nodes are running local clocks
- Local clocks are precisely synchronized to a common wall clock via PTP

  PTPv1 standardized by IEEE in 2002 (IEEE 1588-2002)
  PTPv2 followed in 2008 (IEEE1588-2008)
  PTPv1 and PTPv2 are not compatible!

Skip PTP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PTP – An IEEE Standard

- A standard (IEEE 1588) which describes a protocol for transferring time precisely through data networks
- Precision Time Protocol (“PTP”)

- Current version IEEE 1588-2008 (PTP v2)
- Previous version IEEE 1588-2002 (PTP v1)
- Latest version IEEE 1588-2019 (PTP v2.1) -> Final draft, not yet published

- Accurate (sub-µs) time and frequency transfer
- Already widely used in ethernet based applications
  - Telecom, Power, Finance, Test & Measurement, Industrial automation, …
- Highly generic standard
  - Customizable via PTP profiles

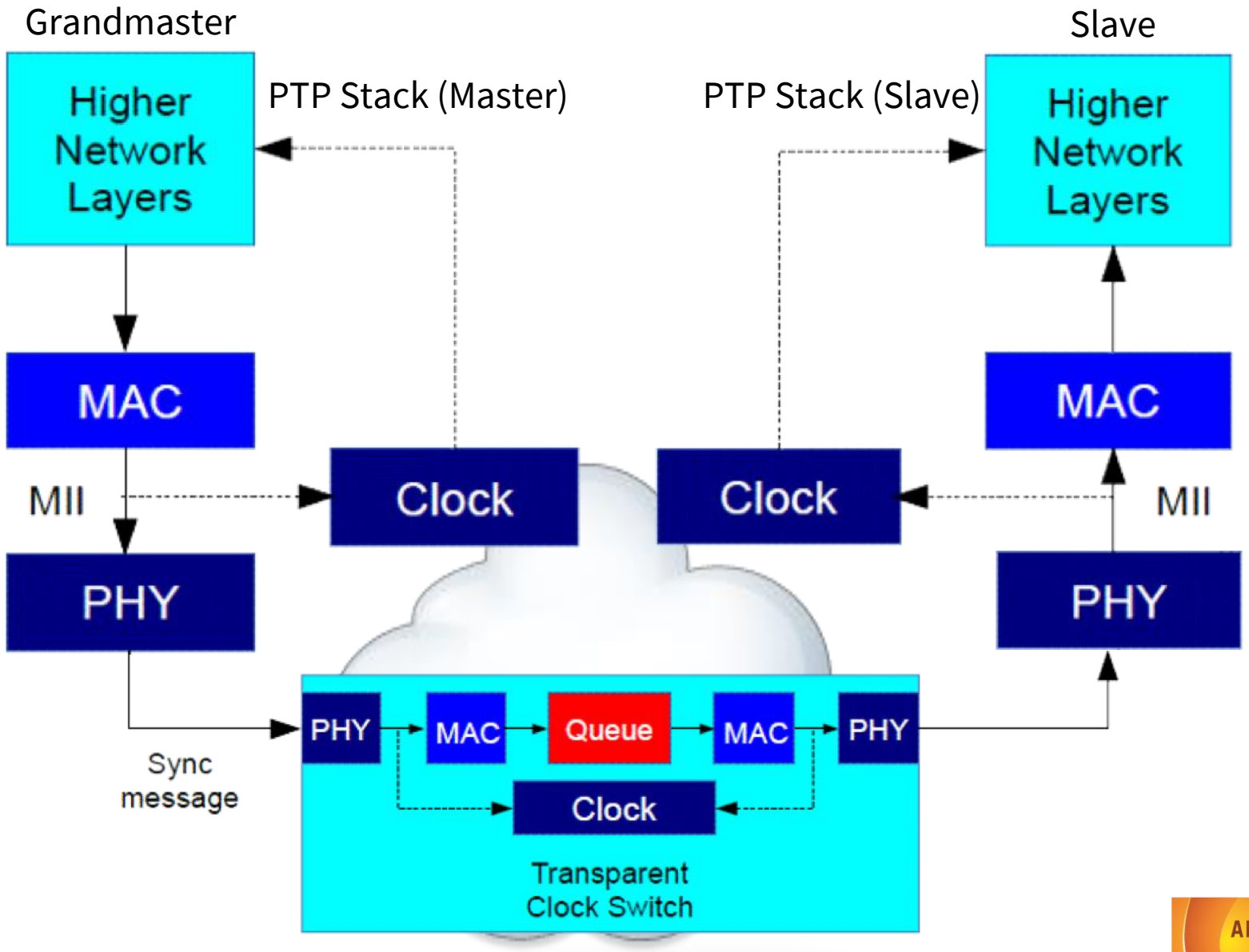
"What makes PTP so precise?"

Answer:

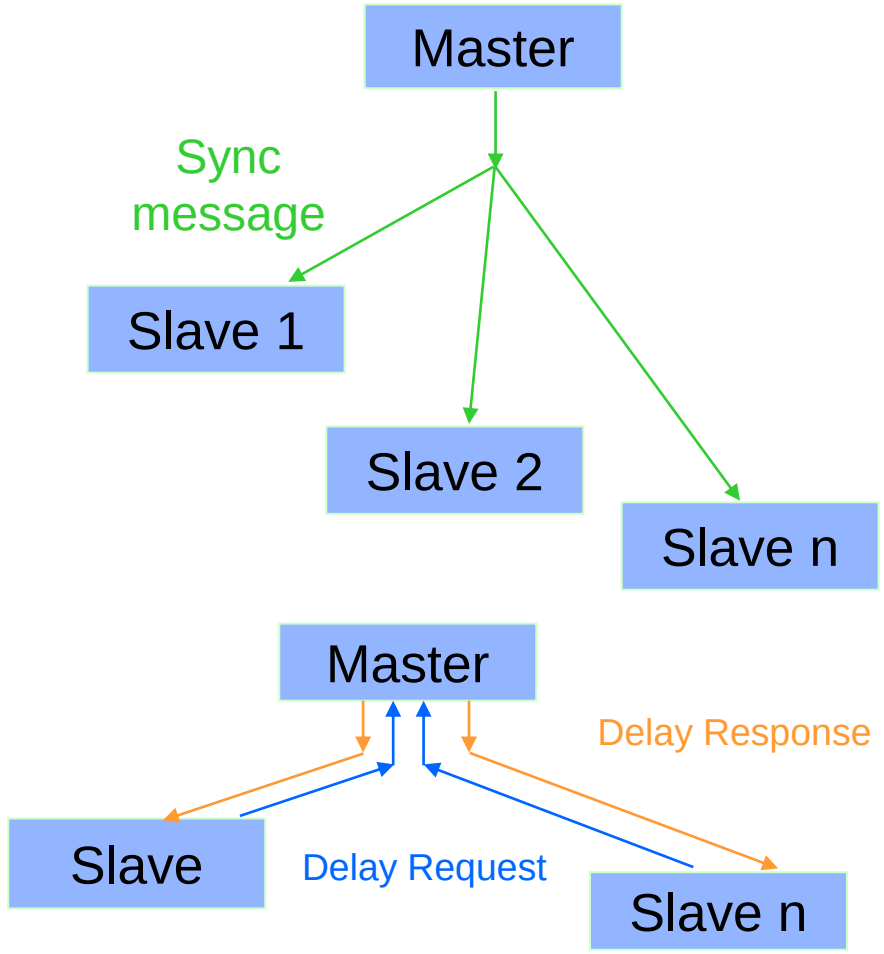
"Hardware timestamping"

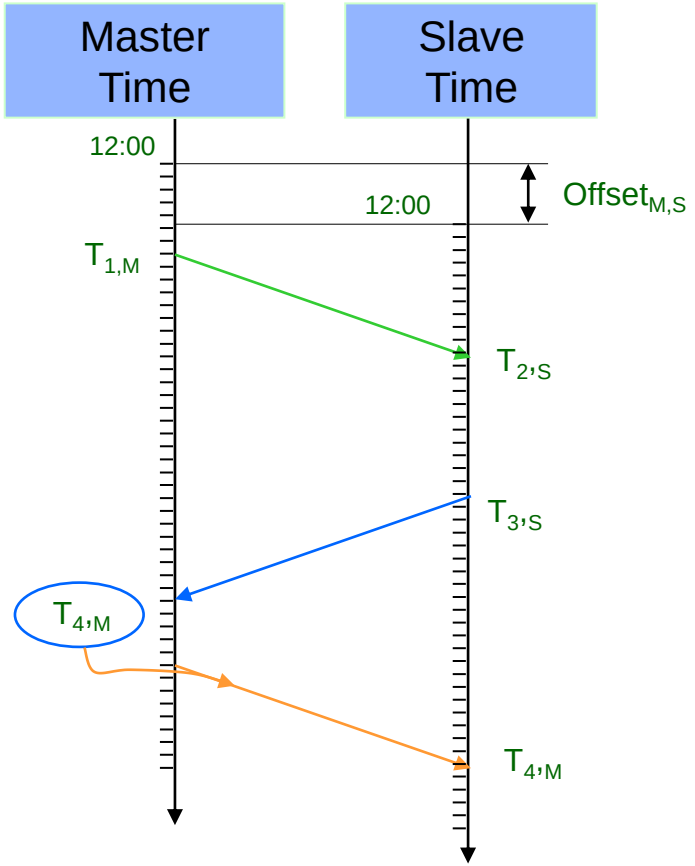
Network Interface Card

MII = Media Independent Interface



Basic Synchronization Principle





$$T_{2,S} - T_{1,M} = T_{2,1}$$
$$T_{4,M} - T_{3,S} = T_{4,3}$$

$$Offset = \frac{T_{2,1} - T_{4,2}}{2}$$

$$Delay = \frac{T_{2,1} + T_{4,3}}{2}$$

1. M → S : SYNC
   „It's roughly 12:03:45.6653776“

2. M → S : FOLLOW-UP
   „When I said it was 12:03:45.6653776,
   it was actually 12:03:45.6658994 !“

3. S → M : Delay Request
   „Tell me when you receive this,
   I store the timestamp when the message leaves!“

4. M → S : Delay Response
   „Got your last message at 12:03:48.6726323“

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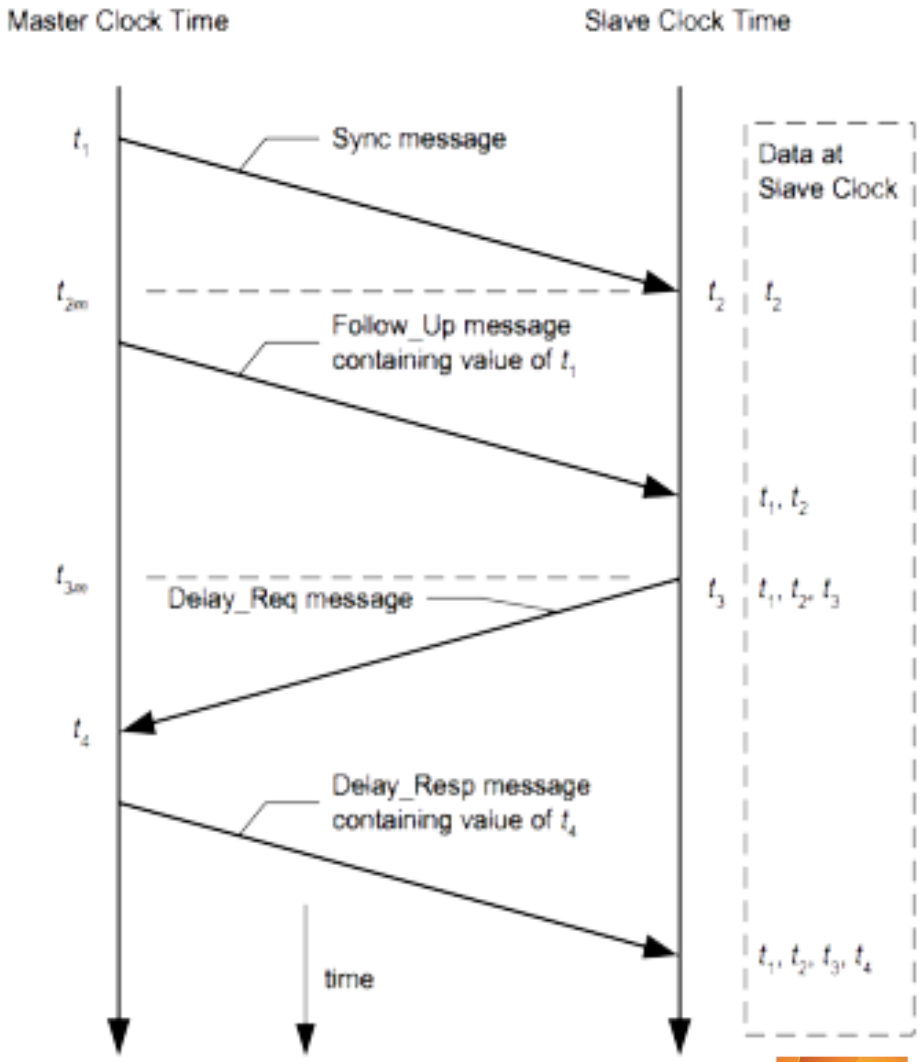
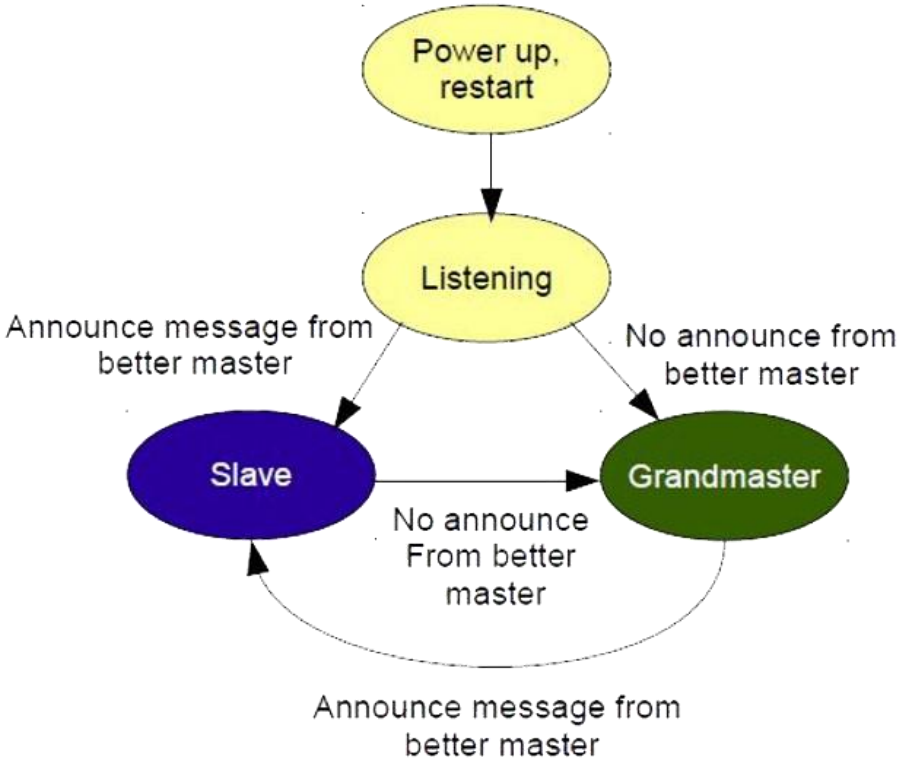


Best Master Clock Algorithm (BMCA)

- Compare own data set with current active master in the following order:
  (upon received ANNOUNCE message):

1. Priority 1 (User Configurable: 0..255)
2. ClockClass (state of the ref clock: 6 = locked to Reference, 7 = in Holdover, 52 = never sync since startup)
3. ClockAccuracy (phase accuracy of the clock: < 100ns, < 250ns, < 1µs, …)
4. ClockVariance (stability of the clock → oscillator dependent, vendor specific)
5. Priority2 (User Configurable: 0..255)
6. Clock UUID (usually based on MAC address of PTP port, lower ID wins BMCA)

PTP – Startup procedure, BMCA



- **Default Clock Class: 248**
- **Clock Class**: >= 128 .. < 255
  → Clock can enter Master or Slave State
- **Clock Class**: < 128
  → Clock can enter Master or Passive, never Slave
- **Clock Class**: 255 („Slave only“)
  → Clock can be Slave Only, never Master

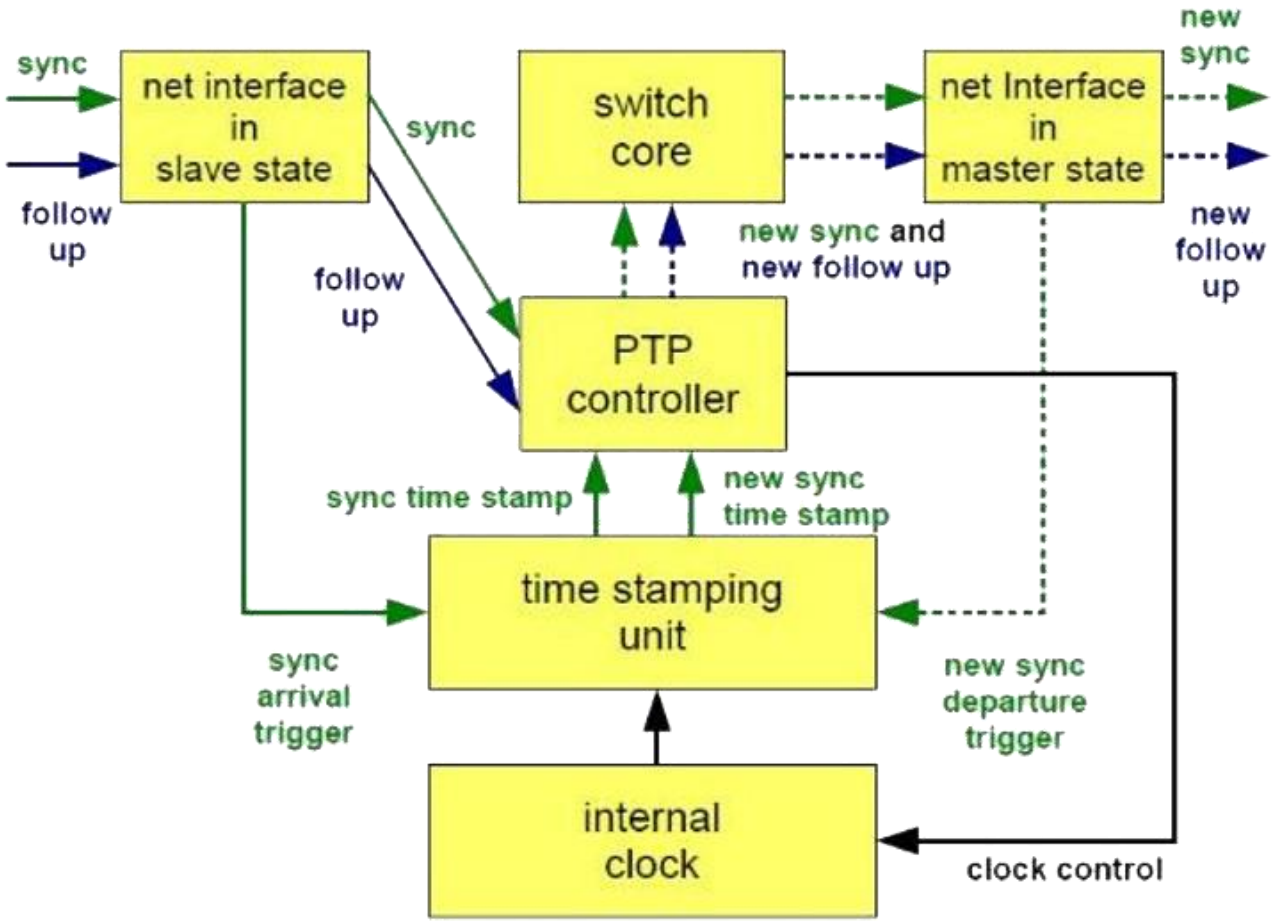
PTP – Planning your infrastructure

- Transmission delay ought to be constant
  - Overprovisioning of network
  - Limits in HW architecture of network devices
  - Can be mitigated by prioritizing PTP traffic

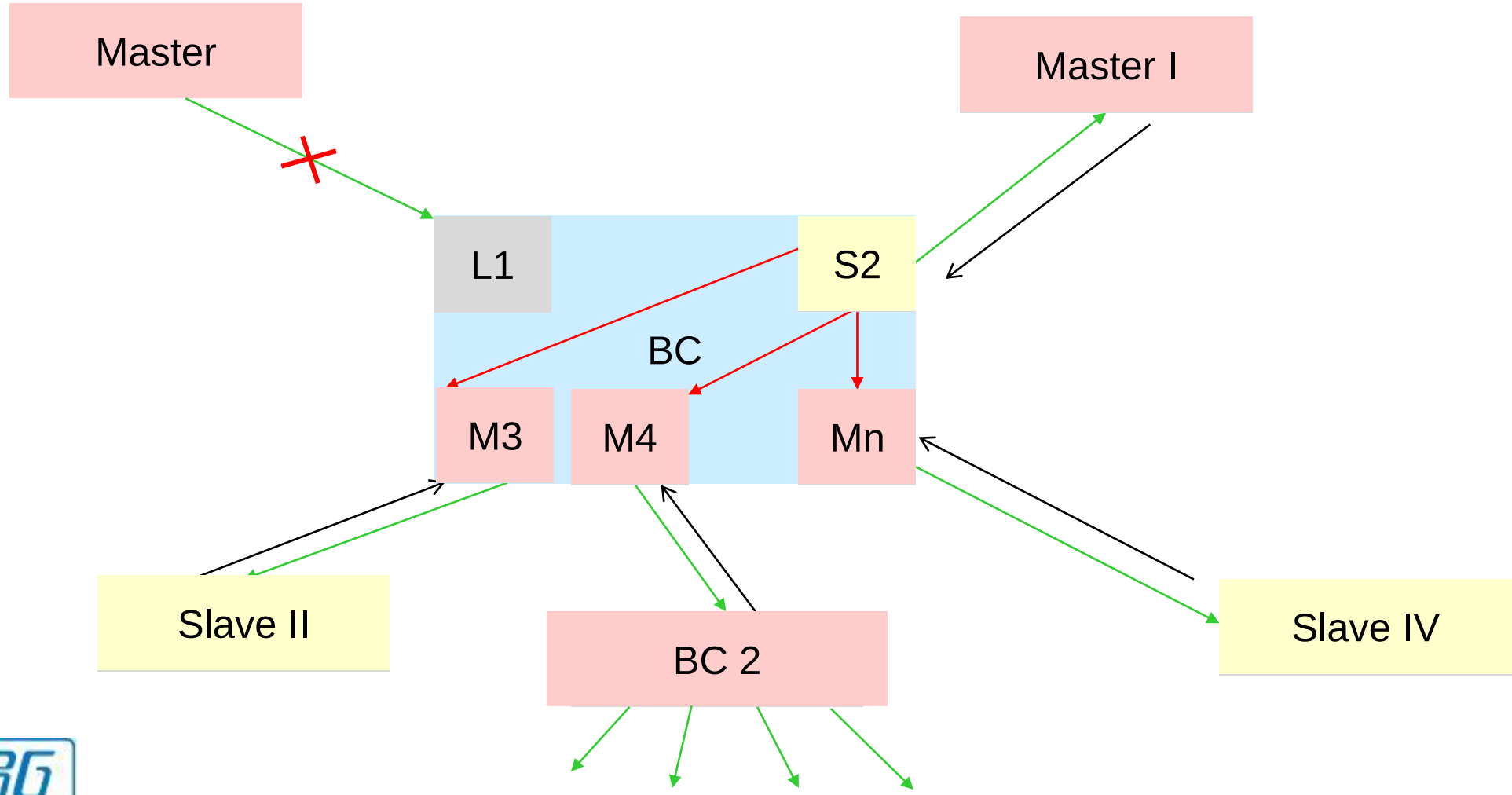
- Careful planning of network architecture and load

- PTP aware network devices
  - Transparent Clocks
  - Boundary Clocks

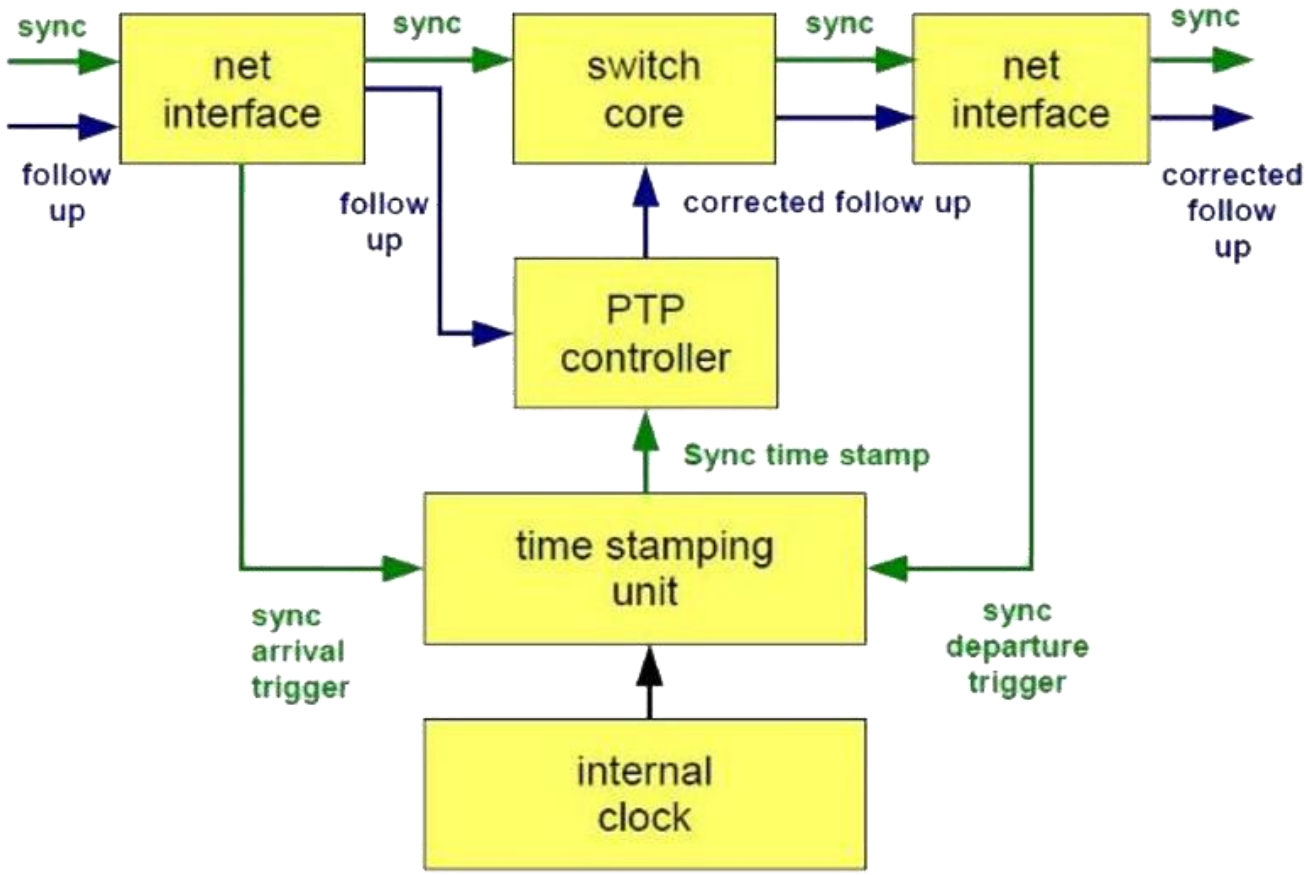
PTP – Boundary Clock – general concept



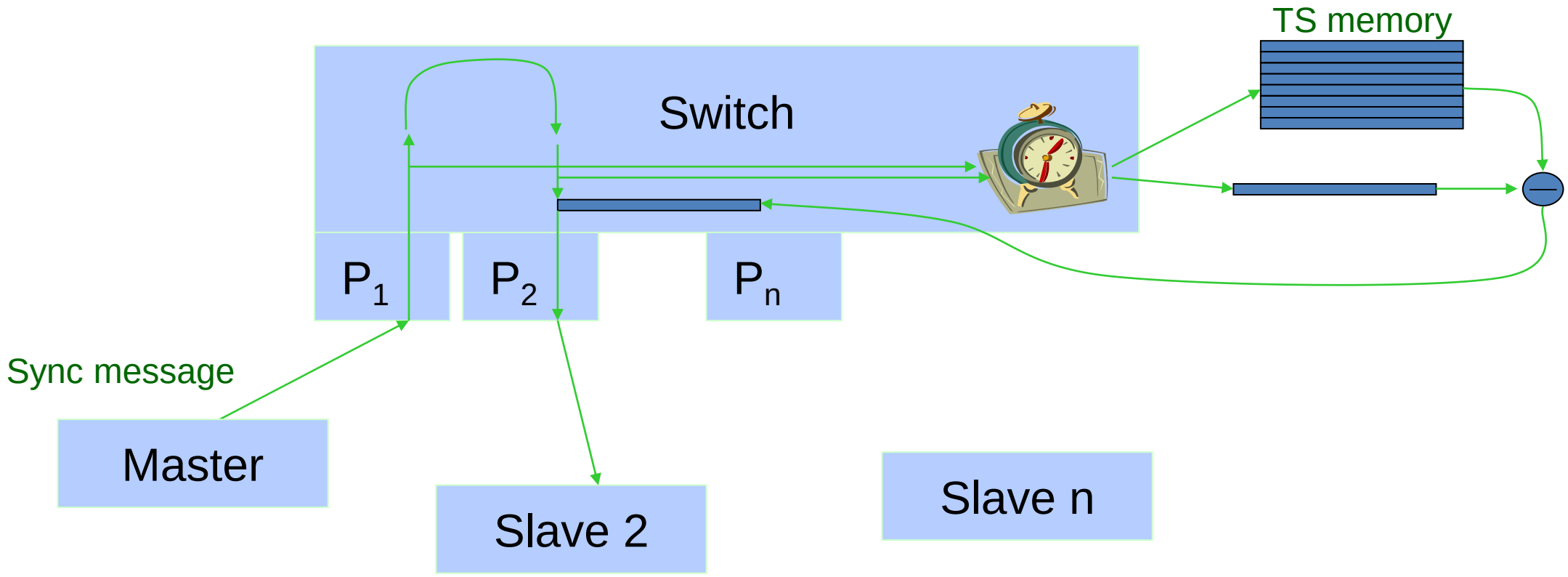
PTP – Boundary Clock – State changes on failover



PTP – Transparent Clock – general concept



PTP – Transparent Clock – signal flow



PTP aware network devices - Summary

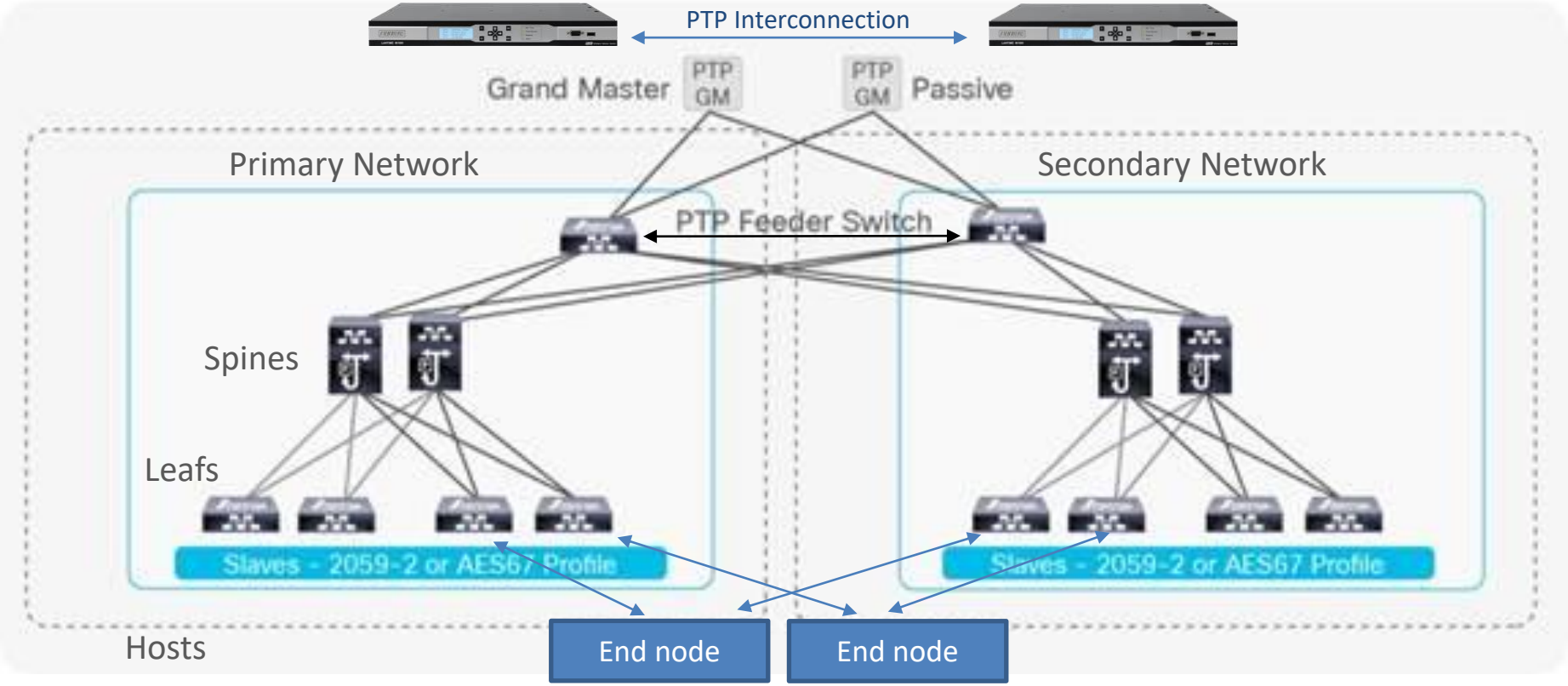
- Boundary Clock (Active PTP Device)
  - The local clock is synchronized to the Grandmaster
  - Every port acts as a PTP node (Ordinary Clock)
  - Time is re-generated and forwarded to all Slaves

- Transparent Clock (Passive PTP Device)
  - Residence time is measured for every PTP packet
  - Timestamps are drawn at ingress and egress.
  - Difference is added to the „Correction Field“

PTP aware network devices – Pros and Cons

- Boundary clocks
  - \+ Good for hierarchical systems
  - \+ Scale well with the number of devices
  - \+ Can translate between different media
  - \- Cascaded Systems require special attention
  - \- Requires continuous monitoring
- Transparent Clocks
  - \+ Simple deployment, minimal monitoring
  - \+ Accuracy independent of network topology
  - \- Scale poorly with the number of devices (Master sees all slaves)

SMPTE ST 2110 – Redundant network according to ST 2022-7



- Duplicated network architecture as per SMPTE ST 2022-7
- PTP Grandmaster are connected via PTP „Feeder Switches“ to the Spines (PTP traffic only)
- End nodes receive duplicated traffic via 2 physical ports
- PTP BMCA in the end node over two PTP slave instances
- Meinberg „PTP Auto“ Interconnection to keep GMs in phase, even on antenna failure(s)

PTP v2.1 – Preview of the next revision

"Don't panic!"

"The working group shall ensure that the resulting draft has the highest degree of backward compatibility possible with the previous edition of IEEE 1588…"

- From the Bylaws of the IEEE 1588 Working Group

What Backward compatibility means:

- New edition device will not break 2008 edition network
- New features are optional
- Old features work as before

Year	Version number	Backward compatible
2002	1	N/A
2008	2	No
2019	2.1	Yes, with v2

PTP v2.1 – Profile Isolation

Table 18—Common message header

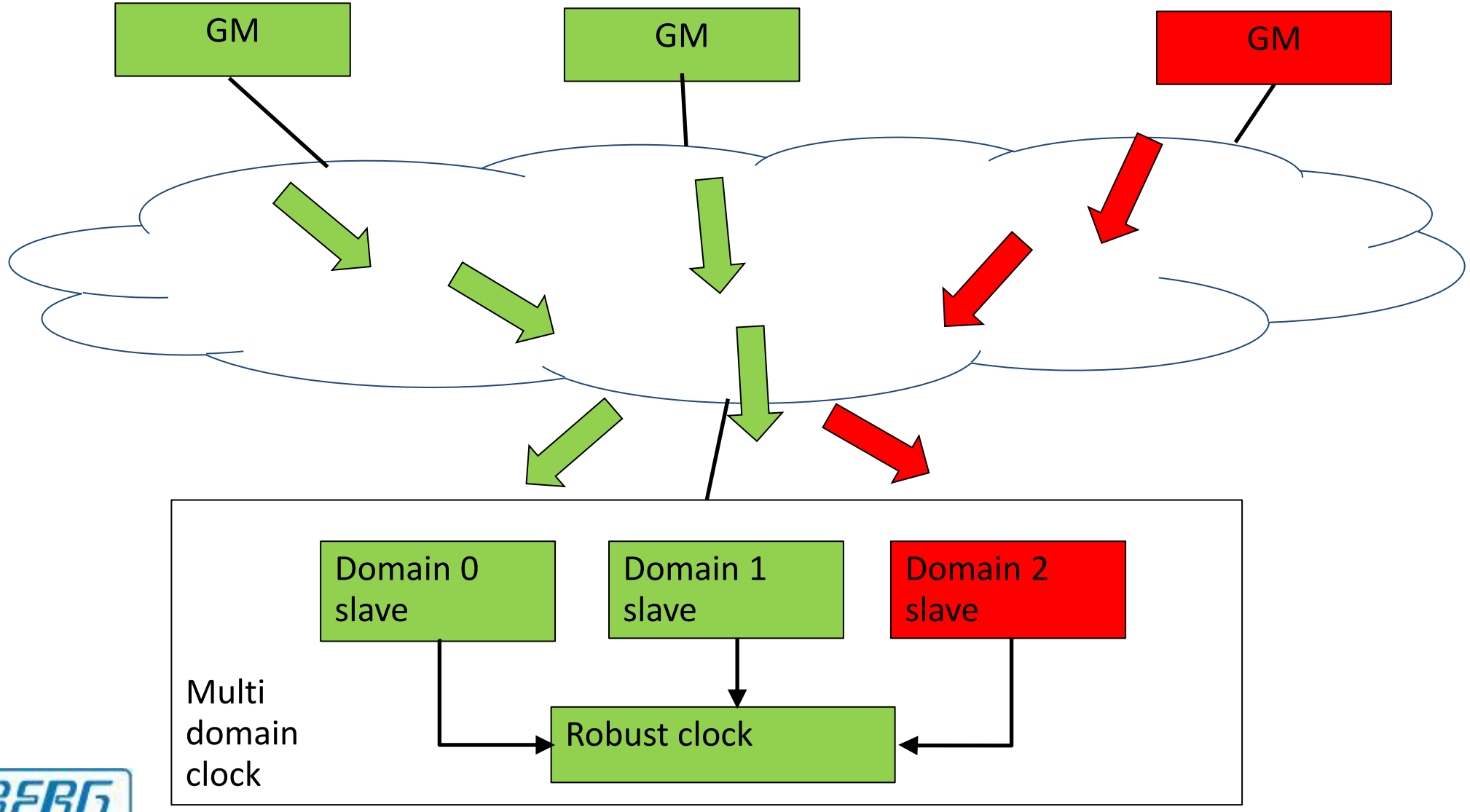
Bits								Octets	Offset
7	6	5	4	3	2	1	0		
transportSpecific				messageType				1	0
reserved				versionPTP				1	1
messageLength								2	2
domainNumber								1	4
reserved								1	5
flagField								2	6
correctionField								8	8
reserved								4	16
sourcePortIdentity								10	20
sequenceId								2	30
controlField								1	32
logMessageInterval								1	33

Table 26—Common PTP message header

Bits								Octets	Offset
7	6	5	4	3	2	1	0		
majorSdoId				messageType				1	0
minorVersionPTP				versionPTP				1	1
messageLength								2	2
domainNumber								1	4
minorSdoId								1	5
flagField								2	6
correctionField								8	8
messageTypeSpecific								4	16
sourcePortIdentity								10	20

SdoId = Standardization development organization identity
→ given to a standards organization
→ allows profile isolation, domain independent

PTP v2.1 – Interaction among domains



PTP v2.1 – Summary of new features

- **Features for robustness and accuracy**
  - Profile Isolation
  - Interdomain interactions
  - Security TLV
  - Standard metrics
  - Slave port monitoring

- **Features of Accuracy**
  - Manual port configuration
  - Calibration
  - Layer-1 syntonization

- **Features for flexibility**
  - Modular TCs (e.g. Special SFPs)
  - Special ports (Timing transfer)
  - Mixed multicast/unicast

Backwards compatibility to V2 remains!
A PTPv2 Slave will sync to a v2.1 master!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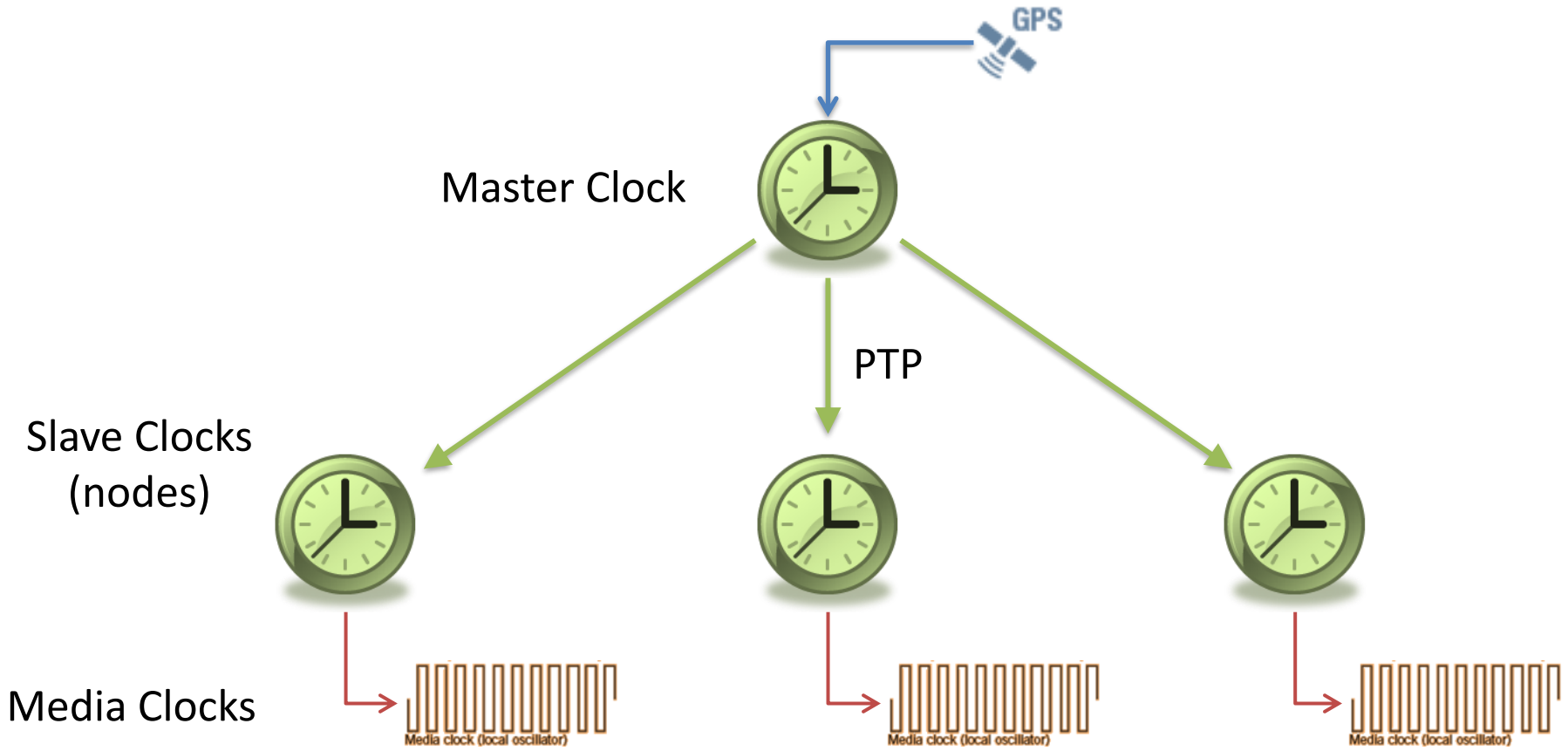
Synchronization & Media Clocks

- All nodes are running local clocks
- Local clocks are precisely synchronized to a common wall clock via PTP
- Media clocks are generated locally from synchronized local clock

Synchronization & Media Clocks



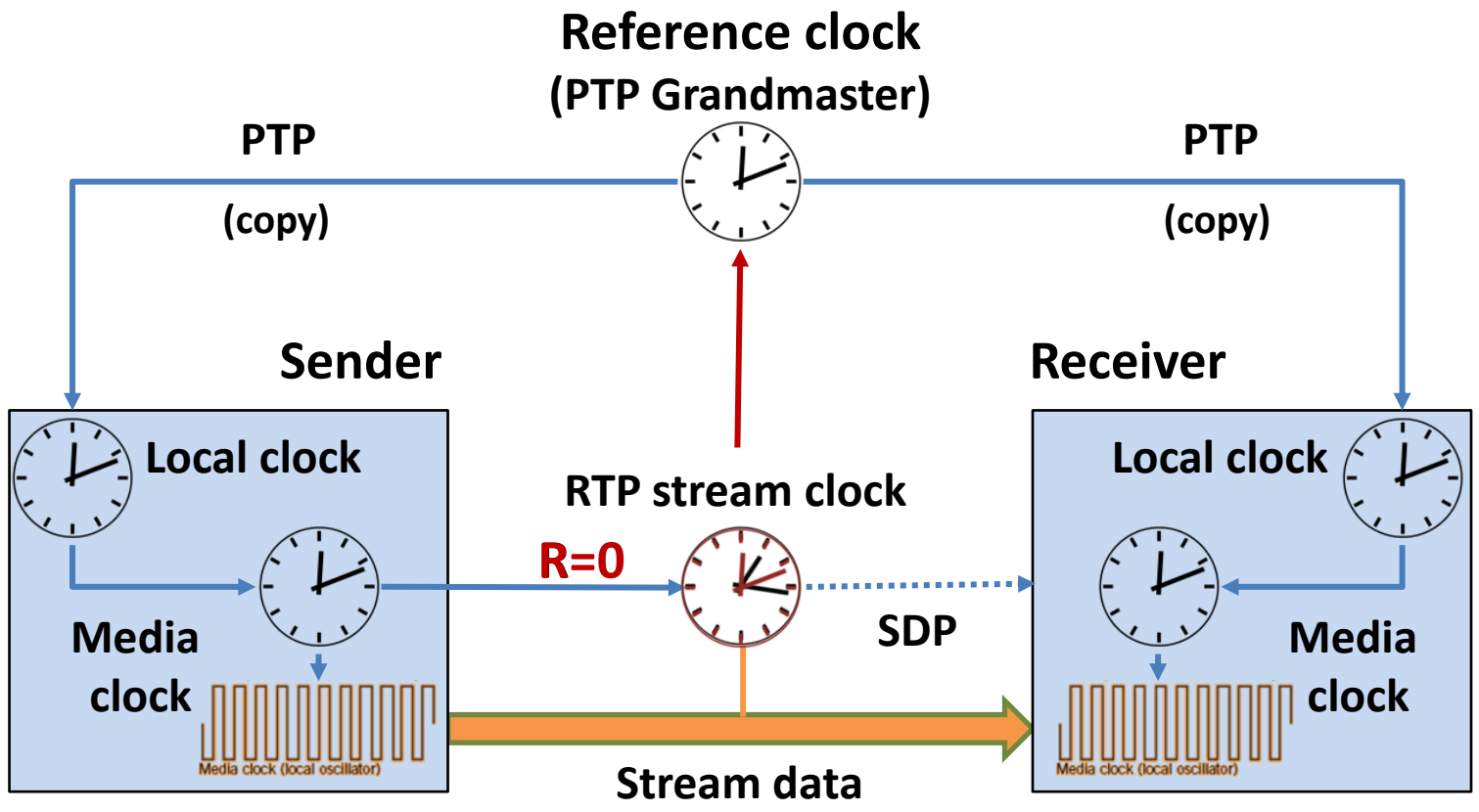
Synchronization & Media Clocks

- All nodes are running local clocks
- Local clocks are precisely synchronized to a common wall clock via PTP
- Media clocks are generated locally from synchronized local clock
- Generation of any desired media clock (sample rate) possible
- Concurrent operation of different media clocks possible
- Phase accuracy of AES 11 (± 5% of sample period) achievable by deployment of PTP-aware switches (BC or TC)
- Synchronization across facilities possible by reference to absolute time (TAI / GPS)
- Essence data (audio samples or video frames) is related to the media clock upon intake - essentially receiving a generation “time stamp” with respect to the media clock

Synchronization & Media Clocks

- 3 type of clocks in the system:
  - Wall clock - provided by Grandmaster
    - local copy of the wall clock in each node
  - Media clock – derived from the local clock (i.e. 48 kHz for audio, 90 kHz for video)
  - RTP clock (stream clock) – derived from the media clock

Synchronization & Media Clocks

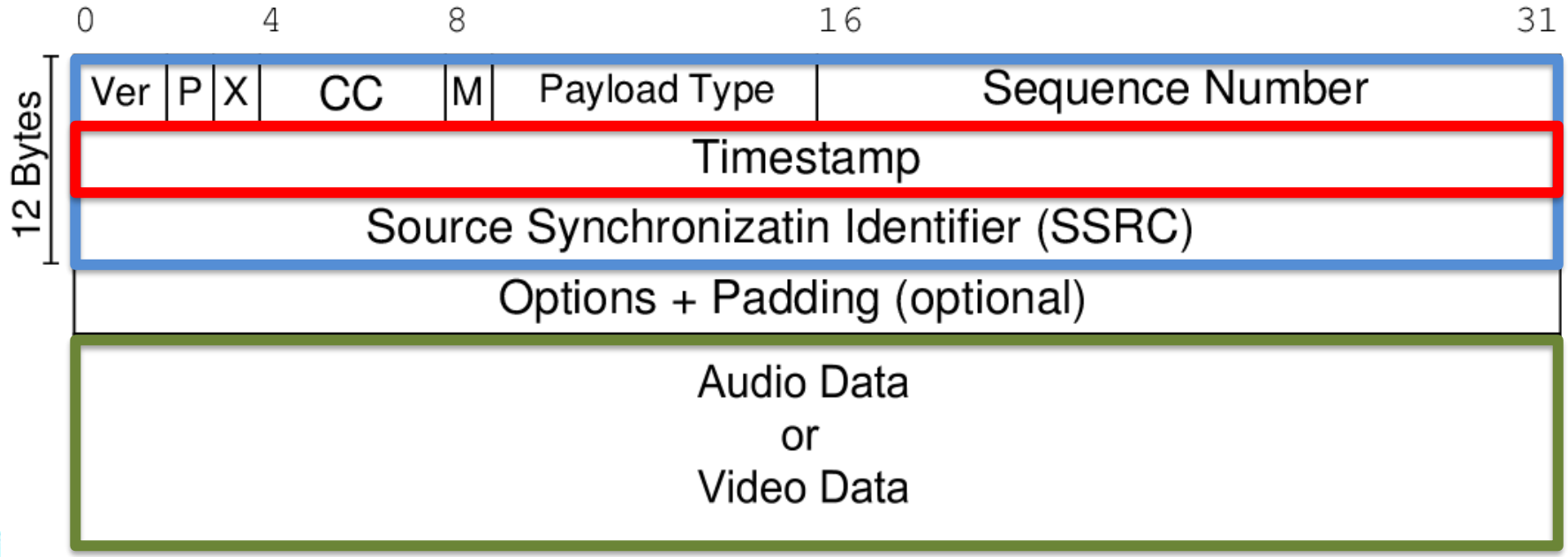


- Offset **R** is established on stream start-up
- **R** may be random to defeat crypto-text attacks
- This offset will be constant throughout the stream's lifetime

- The offset (**R**) will be conveyed via SDP (a=mediaclk:direct=<offset>) **– must be "0" in ST2110**

RTP Packets (Layer 5)

- Consist of RTP header, optional payload headers and the payload itself
- **RTP header** (overhead) = 12 bytes, **RTP payload** (linear audio data) = up to 1440 bytes
- **RTP Timestamp** = **media clock counter** (for linear PCM audio) = 32 bits (4 bytes)
  - ⇨ rollover will occur roughly once per day (~ 1d, 51m, 19s)



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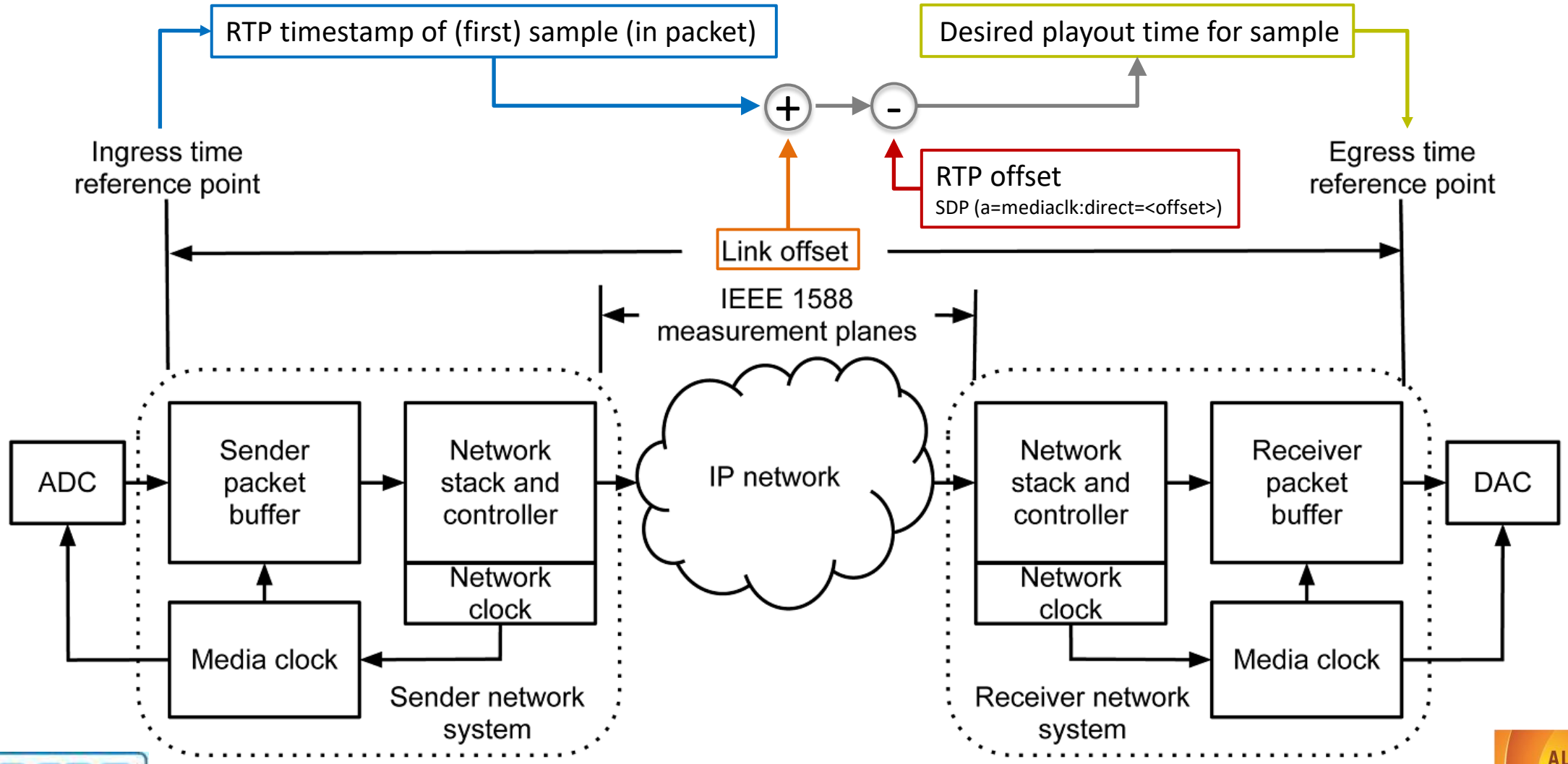
- Fixed / determinable latency by configuring a suitable link offset (“playout delay”)

AES67 synchronization - link offset (latency)



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- Fixed / determinable latency by configuring a suitable link offset (“playout delay”)
- Inter-stream alignment by comparing and relating the time stamps of individual essence data

Production Workflow Timing

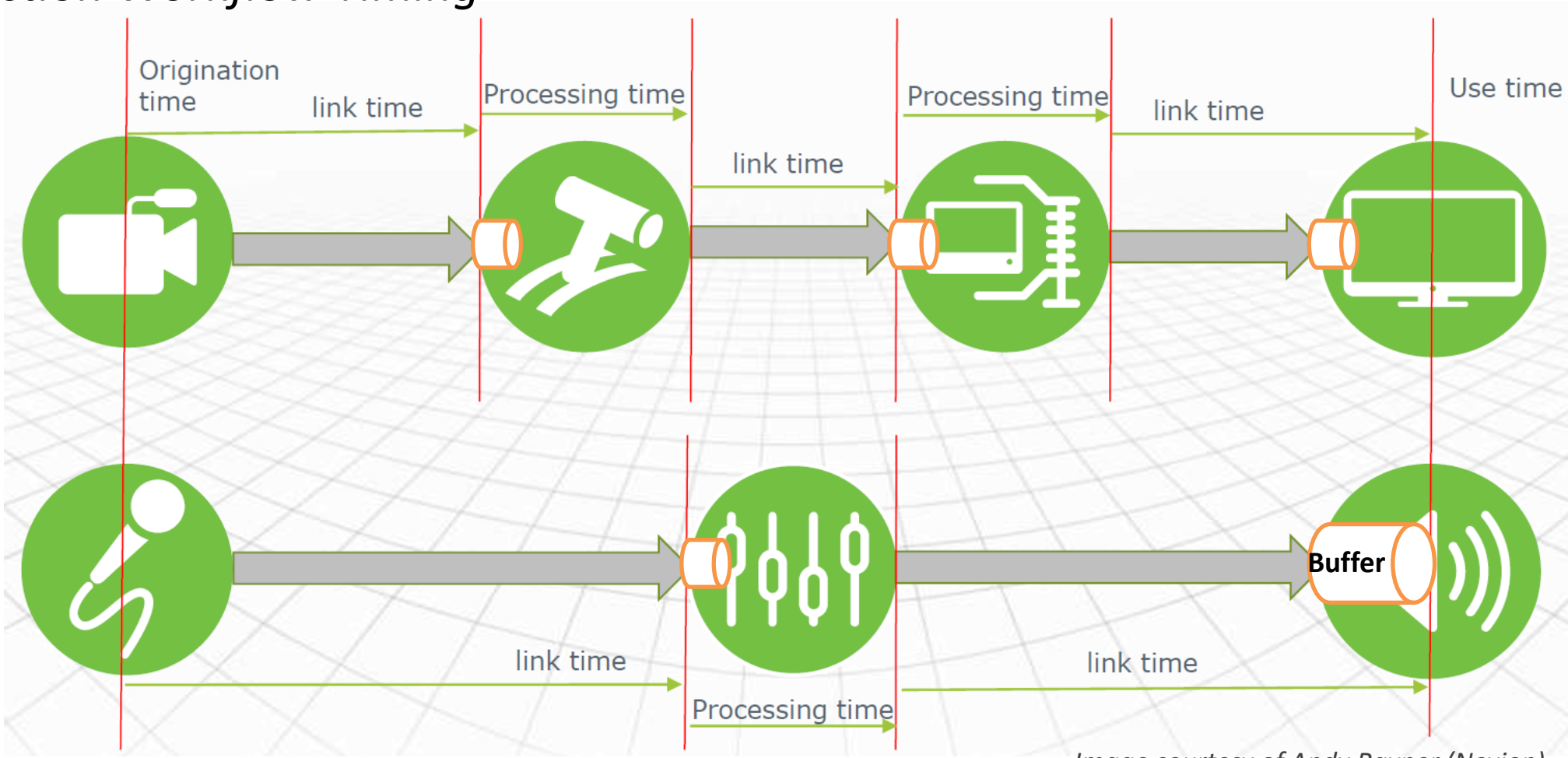

Image courtesy of Andy Rayner (Nevion)

How to synchronize streams across various processing stages

- Problem:
  - Any stream leaving a (processing) device is a new stream
  - New alignment of (processed) essence to wall clock time
  - Alignment of original essence is lost
- Possible solutions:
  - Use of original time alignment for new stream (RTP timestamps adjusted to those of original essence)
    - Offset increases, might be too large for some downstream Rx buffers
    - Which timestamps serve as reference when mixing essence?
    - How does the (processing) host know the exact relationship between ingress and egress essence?
  - Carry origin timestamps as in-band meta data
    - Requires new payload format (audio essence data + audio meta data), or
    - Needs to make use of (experimental) RTP header extensions mechanism (which in turn may result in variable / decreased audio payload segments)
  - Carry origin timestamps as out-of-band meta data
    - Requires new standard (in the works → **AES X242, SMPTE ST2110-41/42, NMOS IS-??**)

How to synchronize streams across various processing stages

- Problem:
  - Any stream leaving a (processing) device is a new stream
  - New alignment of (processed) essence to wall clock time
  - Alignment of original essence is lost

- Intermediate (?) / current solution:
  - Leave alignment task to management layer (i.e. Broadcast Controller)
    - Devices report processing delays to BC (or have fixed / configurable delays)
    - BC configures required Rx delay for subsequent stages (playout delay)

Production Workflow Timing

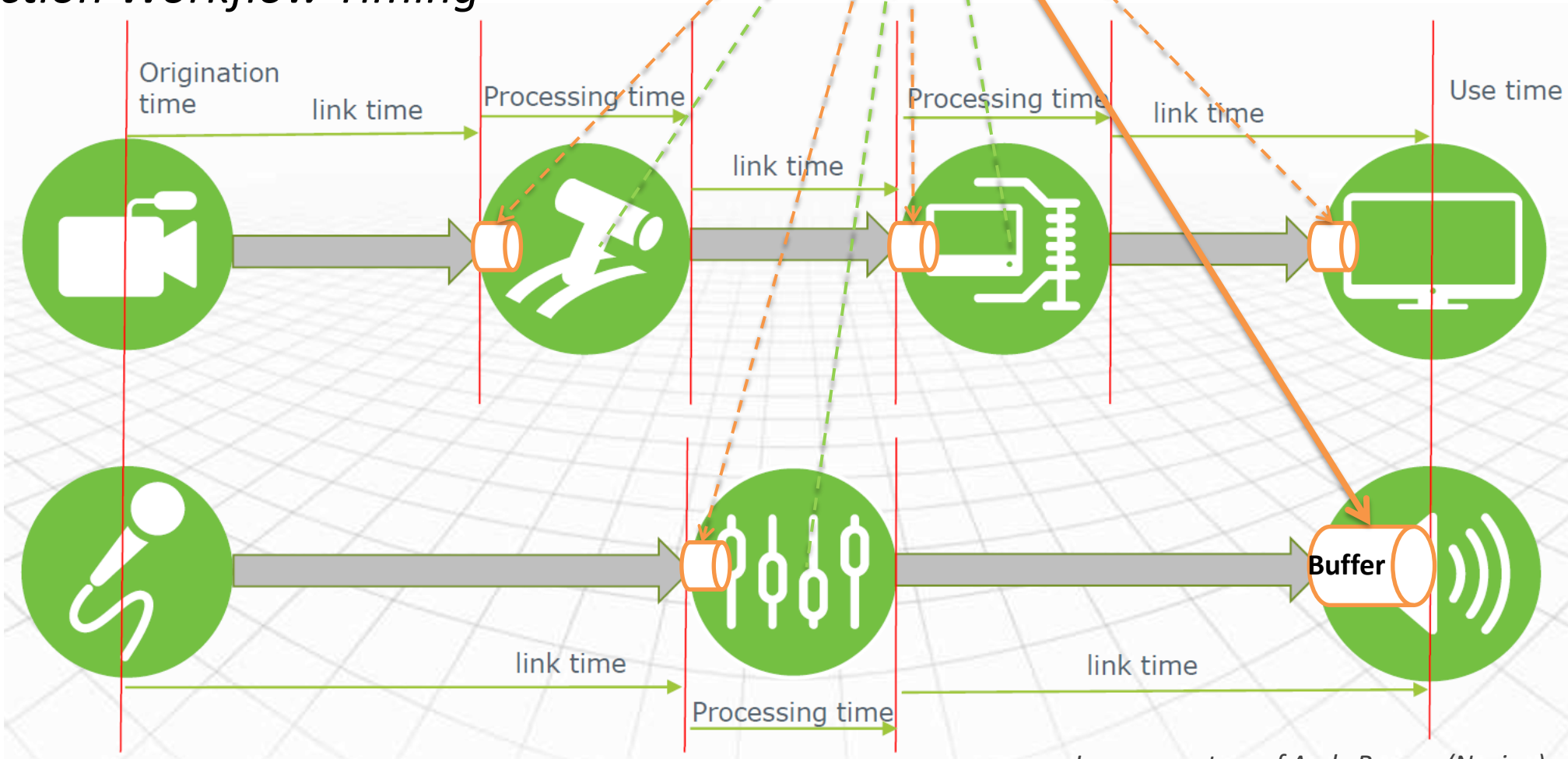

Image courtesy of Andy Rayner (Nevion)

Skip to Q&A

Factors impacting achievable precision

- Grandmaster:
  - Accuracy of clock reference / internal oscillator
  - Availability of GM device (backup)
- Slaves (end nodes):
  - PTP messages frequency (sync, delay_request, announce)
  - Internal clock implementation: filtering (mean value, outlier detection, …), PLL characteristics (slow/fast, static/ adaptive, …), holdover capabilitiy, …
- Network:
  - Topology / size / availability
  - Link speed
  - Mean bandwidth utilization / dynamic traffic situation
  - ⇨ QoS (prioritization of PTP and media traffic)
  - ⇨ Deployment of Boundary and/or Transparent Clocks (BC / TC)
  - ⇨ Redundant networks

PTP Deployment Tips

- Check suitability of network architecture
  - Use structured topologies, leaf-spine recommended, avoid daisy chaining
- Deploy BC or TC, if required (larger networks, high traffic / bandwidth utilization)
- Select / adjust PTP operating profile (PTP Default / AES67 Media / ST2059-2)
- Choose GM device(s)
  - Dedicated device vs. suitable end node
  - Plan for backup / redundancy
- Configure critical PTP parameters (domain, announce & sync message rates, slave-only, priority1 etc.)
- Peculiarity Dante: legacy devices use PTPv1
  - One AES67-enabled Dante device will act as Boundary Clock (PTPv2 → PTPv1)
  - PTP-aware switches may block PTPv1 traffic
  - Dante devices require sync_msg interval <= 2^-2 (no sync on PTP Default profile)

Questions?

More answers…

RAVENNA / AES67 / SMPTE ST 2110 Resources:

www.ravenna-network.com/resources

PTP Resources:

www.meinbergglobal.com/english/info

blog.meinbergglobal.com

RAVENNA 2020 Webinar Series

AES67 Practical: Configuring Devices

Tue, June 16, 2020
15:00 h (CEST)

Claudio Becker-Foss, DirectOut
Andreas Hildebrand, ALC NetworX

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RAVENNA 2020 Webinar Series

AES67 Practical: Configuring Switches

Tue, June 23, 2020
15:00 h (CEST)

Bart Swinnen, Luminex

Nicolas Sturmel, Merging

Andreas Hildebrand, ALC NetworX

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